Fabrication of nanometer-scale side-gated silicon field effect transistors with an atomic force microscope

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The fabrication of nanometer-scale side-gated silicon field effect transistors using an atomic force microscope is reported. The probe tip was used to define nanometer-scale source, gate, and drain patterns by the local anodic oxidation of a passivated silicon (100) surface. These thin oxide patterns were used as etch masks for selective etching of the silicon to form the finished devices. Devices with critical features as small as 30 nm have been fabricated with this technique. © *1995 American Institute of Physics.*

Proximal probes such as the scanning tunneling microscope (STM) and the atomic force microscope (AFM) were originally developed to measure surface properties with atomic precision. More recently, proximal probes have been used to modify nanometer-scale regions of suitably prepared surfaces[1] and, with high-vacuum STM, to manipulate and position single atoms on a surface.[2] This ability to modify and pattern surfaces selectively on these length scales suggests that proximal probes may be useful in the fabrication of nanometer-scale structures, with a precision that may exceed the limits of electron beam lithography and perhaps approach the ultimate limit of atom-by-atom control of the surface.

Proximal probes have been used in various ways to generate patterns of possible use for device fabrication, including exposure of polymeric resists,[3,4] selective oxidation,[5,6] and decomposition of an organometallic compound.[7] Very few of these techniques have gone beyond the writing of test patterns to fabricate even simple two-terminal structures such as metal[3,7,8] or semiconductor[9] wires. However, any future nanometer-scale electronics will presumably require active (gated) structures such as transistors. Most recently, an otherwise conventional large-scale Si MOSFET was fabricated using an AFM in a manner similar to that of Ref. 10 to pattern a 0.1 μm gate made of amorphous hydrogenated Si.[11]

In this letter, we report the use of an AFM to fabricate nanometer-scale side-gated silicon field effect transistors (FETs). Both the source-drain channels and the side gates were patterned by a conducting AFM tip. Under suitable bias between tip and H-passivated Si (100) surface in air, the high local electric field oxidizes the Si surface in the immediate vicinity of the tip.[10] The resulting oxide pattern is transferred into the Si layer (which rests on an insulating layer of SiO_2 for isolation) by selective etches which attack silicon but not its oxides. The devices so fabricated show clear transistor action.

The starting material was lightly doped (1×10^{15} cm^{-3}) *n*-type (100) Si which was ion-implanted with oxygen (180 keV, 2×10^{18} cm^{-2}) and annealed (6 h at 1325 °C) to form a SiO_2 layer 400 nm thick 200 nm below the surface. Such material, called SIMOX, is described in more detail elsewhere.[12] In some cases a second implant and anneal (*P*, 100 keV, 2×10^{12} cm^{-2}; 1 h at 900 °C) was performed to raise the doping of the surface Si layer to 1×10^{17} cm^{-3}. In other cases, the lightly doped SIMOX was thermally oxidized and stripped to produce lightly doped Si surface layers as thin as 40 nm.

Ohmic contact pads for source, gate, and drain contacts were formed on the above materials by liftoff of 2 nanometers (nm) of Cr and 150 nm of Au evaporated into windows in photoresist formed by standard optical lithography. These first level metal contacts were made sufficiently thick to facilitate electrical contact by probes or wire bonding. A second level of 2 nm Cr and 15 nm of Au was patterned over the first level to form an etch mask for fingers from the source, gate, and drain contacts to the active regions of the device to be patterned by AFM. The second layer was made thin so that the AFM tip could scan smoothly over the metal edge onto the Si surface; otherwise, the pyramidal shape of the tip would prevent exposure near the metal edge.

Any organic contamination from the optical lithography was removed with solvents and ultraviolet light-generated ozone. The surface was then passivated by immersion in 10% HF for 60 s (which strips any native oxide and terminates the surface bonds with a dihydride layer) and blown dry. This passivating hydride layer is robust and can protect the surface for days unless exposed to heat or chemical contamination.[6]

The source, gate, and drain geometries were patterned with an AFM probe composed of a pyramidal Si_3N_4 tip on a cantilever. The AFM probe was made electrically conducting by coating it with a 30 nm layer of evaporated Ti, which allows a bias to be applied between the tip and the scanned surface.[10] The Ti layer is mechanically and electrically stable, even under bias in contact with a conducting sample. Biasing the tip in contact with a H-passivated Si surface in air creates a local high electric field which strips the H-passivation and grows a thin oxide layer in the vicinity of the tip.[6]

The device patterns were written as follows. The surface was scanned by force feedback and the resulting image used to align the tip to the center of the active area between the source, drain, and gate fingers. The tip was then moved to the thin metal source finger, the exposing bias was applied between the tip and the sample (4–6 V, tip negative), and the

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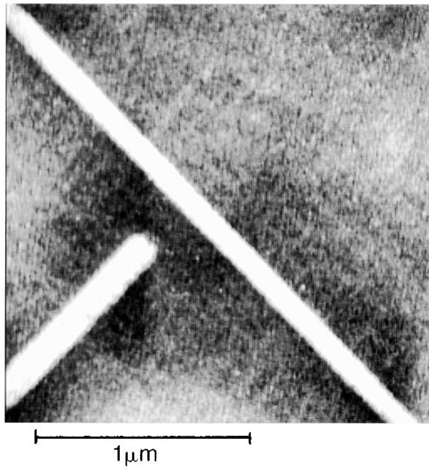

FIG. 1. AFM image of a latent oxide device pattern (prior to etching) imaged with the same tip used to write the pattern immediately after it was written. The source-drain channel pattern is the diagonal line. The side gate oxide line approaches from lower left. Vertical scale (black to white) is 2 nm. The oxide pattern height is ~1.5 nm.

tip was scanned slowly (1–10 μm/s) across the surface from the source to the drain finger. This formed a thin line of surface oxide between the source and drain fingers. Next, an oxide line was drawn from the gate finger to a point near the source-drain line to form the gate pattern.

At this point the written oxide pattern was imaged with the AFM tip. Any defects could be repaired by further oxidation of those regions which were not sufficiently exposed. One advantage to using a conducting AFM instead of a STM for the exposure derives from the fact that for AFM the exposure mechanism (applied bias) is decoupled from the feedback control (contact force). This decoupling allows the repeated imaging of a patterned surface without risk of further exposure.[10] With STM, reimaging the pattern risks further exposure.[6] Figure 1 shows the AFM image of a typical oxide device pattern taken immediately after it was written, and imaged with the same tip used to write the pattern. The height of the oxide pattern above the Si surface is ~1.5 nm.

The sample was next etched in warm (70 °C) hydrazine, which etches Si but not its oxides. The hydrazine removes all the surface Si unprotected by the oxide pattern or the metal masks down to the buried oxide layer, which acts as an etch stop. Figure 2 is a SEM image after hydrazine etching of a single-gate structure fabricated on a top Si layer 40 nm thick. The wire between source and drain is a conducting channel isolated from the substrate by the buried layer of implanted oxide. The source-drain wire shown in Fig. 2 is ~30 nm wide by 40 nm high by 6 μm long. The side gate is a wire 220 nm wide connected at one end to a contact pad and at the other end separated by 160 nm from the source-drain wire. The gate wire in Fig. 2 was purposely made wide and well-separated from the channel wire. Gate wires as narrow as 35 nm with separations of 40 nm from the channel wire have been fabricated. Because liquid etches such as hydrazine generally produce no better than a one-to-one ratio of wire height-to-width, the minimum wire width achievable depends not only on the minimum width of the oxide pattern that can be written but also on the thickness of the layer to be

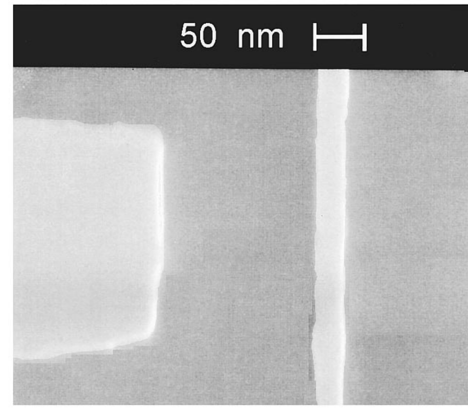

FIG. 2. Scanning electron micrograph of the active region of a side-gated transistor after etching in hydrazine. The width of the source-drain channel (vertical line in picture) is ~30 nm. The gate approaches from the left.

etched. Higher aspect ratios may be achieved through directionally selective etch techniques.

The measured electrical resistances of these wires (both thick heavily doped and thin lightly doped) are higher than expected from the bulk resistivity and the wire dimensions. We attribute this increased resistance to a density of surface states on the exposed walls of the wires sufficient to deplete wires of these dimensions and doping levels. This depletion effect can be counteracted by a positive bias on the substrate, driving the *n*-type wire (which rests on a layer of SiO_2) into accumulation. We observe that about 40 V of backgating is sufficient to restore the conductance of the channel wires. This amount of back-bias implies a surface state density on the order of 10^{12} cm^{-2}, a reasonable value for an unprotected silicon surface.[13]

With the source-drain channel wire backgated into accumulation, the side gate can be biased negatively to pinch the source-drain channel near the side gate into depletion. Figure 3 shows the transistor characteristic of a device (channel dimensions 300 nm wide by 200 nm high, doping 1×10^{17} cm^{-3}) backgated +40 V into accumulation and depleted by a single side gate. The side gate bias ranges from 0 V to −7

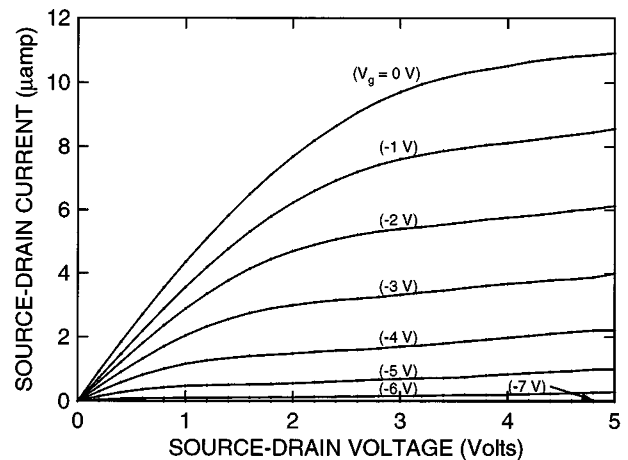

FIG. 3. Drain current vs drain voltage for various side-gate biases (ranging from 0 to −7 V in −1 V steps) for a side-gated Si transistor fabricated by AFM lithography.

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V in −1 V steps. Similar transistor characteristics have been observed for devices made from the thin (40 nm) lightly doped (1×10^{15} cm^{-3}) material with source-drain wires as narrow as 30 nm but with correspondingly reduced currents because of the smaller size and lower doping. These thin lightly doped devices can by increased backgating be driven further into accumulation, achieving currents as high as 5×10^{-7} A. However, in comparison with devices on the thick heavily doped material, these thin lightly doped devices show drifts and variabilities in the current which we attribute to the dominance of surface effects on such small structures.

The sensitivity of small (and especially lightly doped) devices to the surface is not unexpected. This is a general problem which will confront any nanometer-scale device with exposed surfaces, since in this size regime such structures can be viewed as mostly surface. There are various standard methods for protecting exposed surfaces, including oxide growth, encapsulation, hermetically sealed packaging, and other processing techniques which may help to control this sensitivity to the surface.[13]

The design of the structures shown here was optimized for ease of fabrication, not for device performance. In addition to steps to address the problems arising from the exposed surface discussed above, several obvious improvements can be made. The channel resistance can be significantly reduced by replacing the long thin channel wire with a wide geometry which tapers to a thin wire only in the region near the gate. Gating action can be increased by using a split-gate geometry to modulate from both sides of the channel instead of one. The thin material can be heavily doped like the thick material, which would allow it to carry a significantly higher current and also reduce its sensitivity to surface charges. We are currently investigating several of these improvements.

The side-gated FET structures discussed here are uncommon for silicon (where MOSFETs are the standard for present technology), but are used in compound semiconductor devices such as quantum point contacts. Side-gated FETs offer some intrinsic advantages over conventional device designs, including an inherently low gate-channel capacitance.[14] Low capacitances are essential to the operation of devices such as Coulomb blockade and single electron tunneling structures. Coulomb blockade effects have recently been reported in SIMOX structures made by conventional electron-beam methods.[15] In addition, the exposed surface of the active area of side-gated devices (which makes them sensitive to surface effects discussed above and would normally be considered a drawback) affords the possibility of further modification of device properties. Proximal probe manipulation may allow tailoring of the surface of the active area to near-atomic precision. In suitably thin structures, or in structures with the charge carriers close to or at the surface, such precise surface control may give a corresponding degree of control over the transport properties. The surface modification techniques utilized here are uniquely suited for the fabrication (and further modification) of extremely small closely spaced structures. As an example of the sizes now attainable, Lyding[16] has recently used a high-vacuum STM to write 1 nm wide, 1 monolayer thick oxide lines spaced on a 3 nm pitch on a Si surface. Optimization of proximal probe writing and subsequent pattern transfer techniques may allow the fabrication of structures with critical dimensions below the limits of conventional electron beam lithography, and perhaps reaching the atomic-level resolution already achieved by proximal probe imaging and single-atom manipulation.

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